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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,647	10/08/2003	Jung Pill Kim	2003P5259US	6096

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,647	KIM ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7,10-13,15-22 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7,10-13,15-22,25 and 27* is/are rejected.

7)☒ Claim(s) *26 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03-21-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 04-07-05 has been received and entered in the case. New ground of rejections necessitated by the amendment is set forth below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 5, 6, 7, 10-12, 13 and 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 1, the recitation "the reference voltage" on line 16 is indefinite because it is not clear as to this " the reference is the same or different than the "a reference voltage" on line 6. On line 6, the "a reference voltage" is the reference voltage supplied to the voltage divider (244). The "reference voltage" on line 16 is the reference (Vref-ext) applied to the voltage comparator (246). The same rationale is applied to the " the reference voltage in claims 7, 13.

Claims 5, 6, 10-12 and 15-20 are indefinite because of the technical deficiencies of claims 1, 7 and 13.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office

(a) A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Allgood et al. (USP. 4,384,277).

Regarding claim 21, figure 2 of Allgood shows a method for adjusting a level of a voltage at an output node, the voltage being generated internally to an integrated circuit device, the method comprising:

providing a voltage dividing circuit with a plurality of serially connected resistors;

supplying the voltage dividing circuit with a reference voltage, resulting in a different voltage level at nodes of the voltage dividing circuit formed between the serially connected resistors (136-166);

providing a plurality of switches (172-202), each switch configured to selectively couple the output node to a single node (76) of the voltage dividing circuit; and

providing one or more switches (204, 206) in parallel with one or more of the resistors of the voltage dividing circuit, each to selectively bypass the one or more resistors.

Regarding claim 22, figure 2 of Allgood shows a trimming circuit comprising a plurality of switches (172-202), a voltage divider (136-166) and the additional switches that are coupled in parallel with the resistors are switches (204) and (206).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allgood et al. (USP. 4,384,277).

Regarding claim 25, figure 2 of Allgood includes all the limitations of claim 25 except for the limitation that the voltage dividing circuit is used in a memory device comprising a peripheral circuitry, a plurality of memory cells. However, it is well known that a voltage divider is a circuit commonly used to divide a reference or a supply voltage into different

voltages for supplying input signals to other circuits. Therefore, it is obvious to an artisan having skills in the art that the voltage divider circuit of Allgood can be used in a memory device comprising a peripheral circuitry, a plurality of memory cells for providing different divided voltages derived from a single voltage source.

Regarding claim 27, figure 2 of Allgood includes all the limitations of claim 27 except for the limitation that the voltage dividing circuit is used in a memory devices comprising a peripheral circuitry, a plurality of memory cells and the control signals are stored in a plurality of non-volatile memory elements However, it is well known that a voltage divider is a circuit commonly used to divide a reference or a supply voltage into different voltages for supplying input signals to other circuits. Therefore, it is obvious to an artisan having skills in the art that the voltage divider circuit of Allgood can be used in a memory device comprising a peripheral circuitry, a plurality of memory cells for providing different divided voltages derived from a single voltage source.

The control signals (b4-b7) are PCM signals (col. 7,lines 38-43). Figure 4 of Iwamoto shows that the PCM data can be stored in a non-volatile memory element such as ROM (col.9, lines 42-43). Therefore, it would have been obvious to an artisan having skills in the art to store the PCM data (b4-b7) in a ROM device for preserving the data when the power is turned off.

Allowable Subject Matter

Claims 1, 5, 6,7, 10-12, 13 and 15-20 are allowed because the prior art (4,384,277) fails to teach or suggest a method for adjusting a level of a voltage at an output node comprising generating the control signals as a function of states of one or more non-volatile storage elements, wherein the states are determined based on an output of a voltage comparator comparing the voltage at the output node to an external reference voltage as called for in claim 1; a trimming circuit having a comparator for comparing the voltage at the output node to an external reference voltage as called for in claims 7 and 13.

Claims 26 and 28 are objected to because the prior art (4,384,277) fails to teach or suggest a memory device comprising fuses for generating control signals for the switches as called for in claims 26 and 28.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
06-18-05

TUAN T. LAM
PRIMARY EXAMINER